ABSTRACT OF THE DISCLOSURE

The present invention provides a clock multiplying PLL circuit capable of suppressing jitters with a simple configuration and shortening a lockup time. The clock multiplying PLL circuit (1) comprises a VCO (40) for outputting an output clock signal (ST), first through n-th dividers (51 through 5n) for dividing the output clock signal (ST) and thereby outputting first through n-th divided signals (SD1 through SDn), a DLL (60) for generating first through n-th reference clock signals (SB1 through SBn) different in phase from one another using a reference clock signal (SR), and first through n-th phase comparators (11 through 1n) for comparing phases of i-th reference clock signals (SBi) and i-th divided signals (SDi) (where i: an integer of 1 to n). An oscillation frequency of the output clock signal (ST) of the VCO (40) changes based on the results of comparisons by the first through n-th phase comparators (11 through 1n).